Experiment NO. - 03

Characteristics of Junction Field Effect Transistor (JFET)

Object :-

To study of depends of output drain current on gate source voltage (V_{GS}).

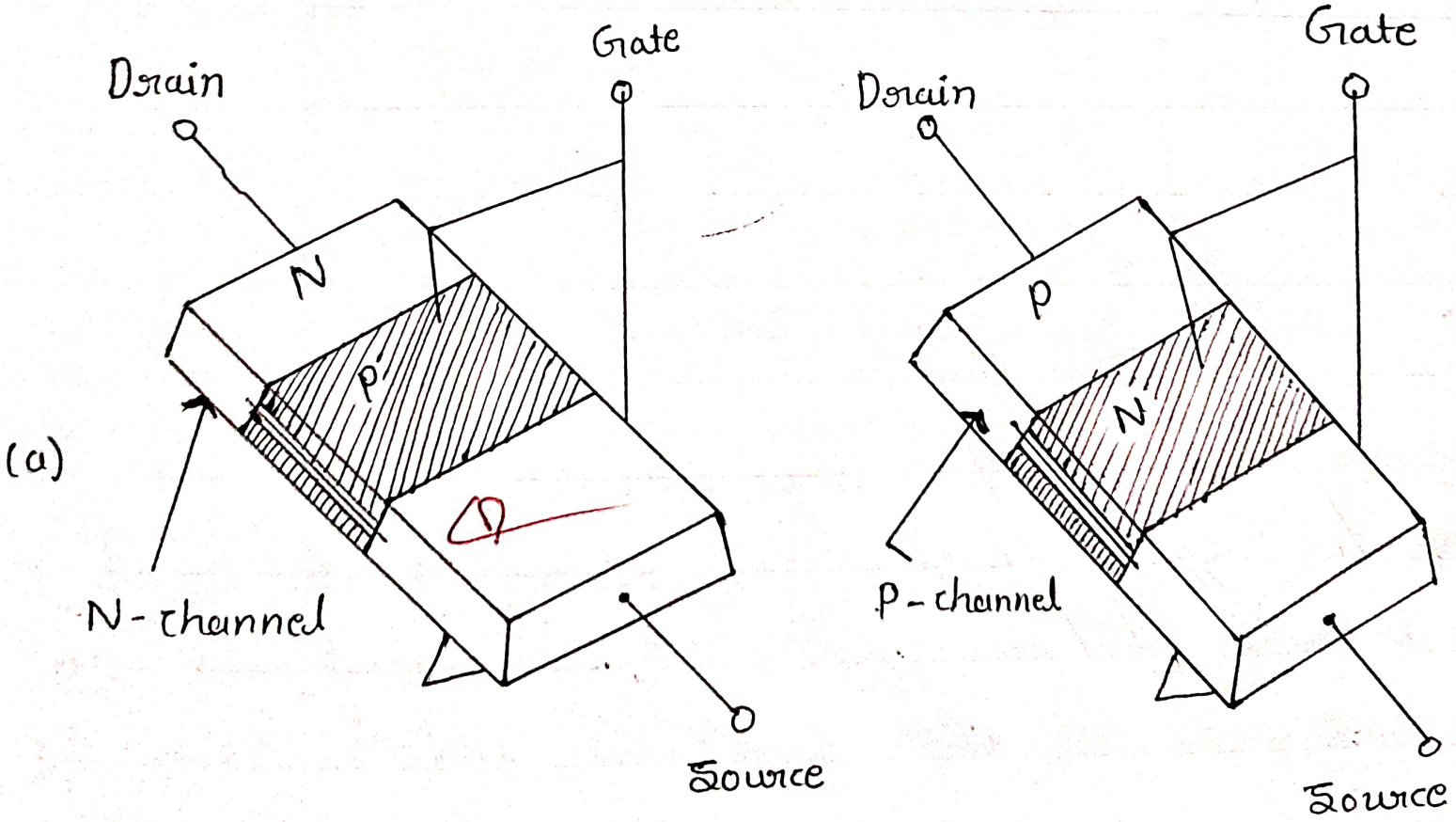
Apparatus required :-

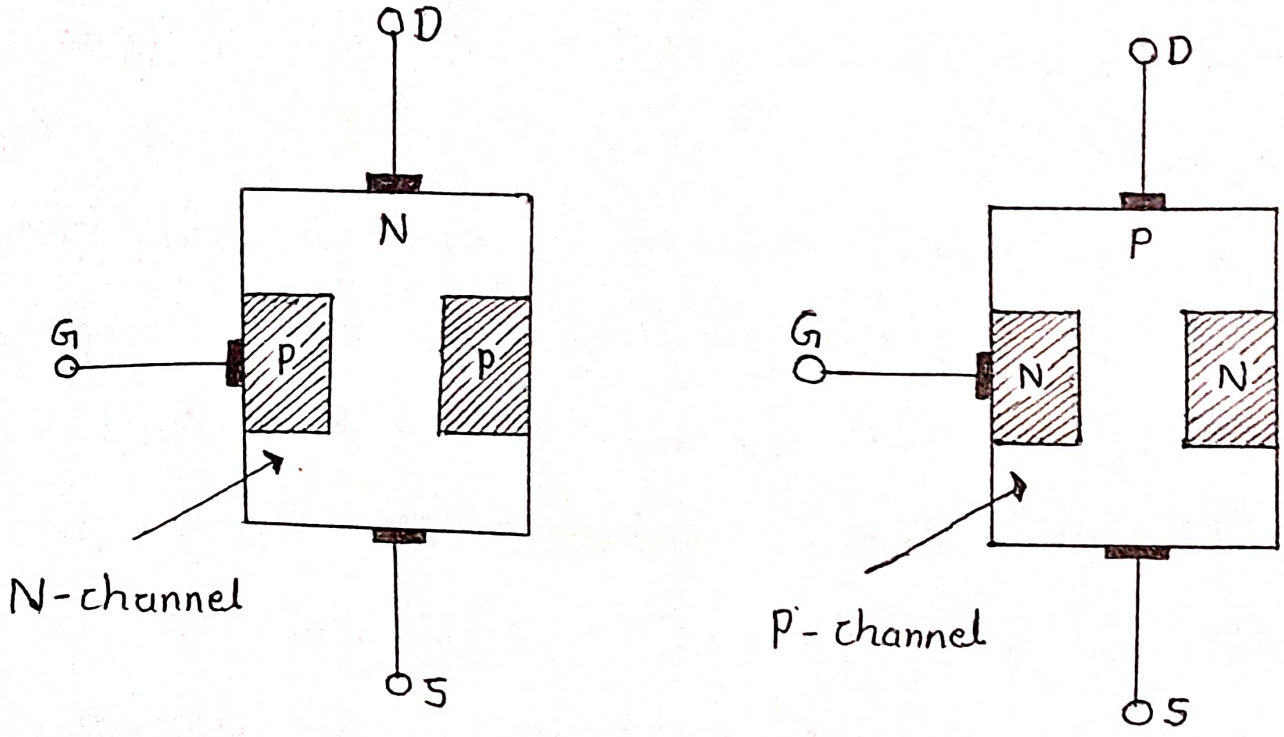
JFET (BFW10), Bread board, Regulated Power Supply (0-2V) and (0-12V), Ammeters (0-20mA), Voltmeter V_1 (0-2V), Voltmeter V_2, (0-10V), Connecting wires (Single strand).

Principal :-

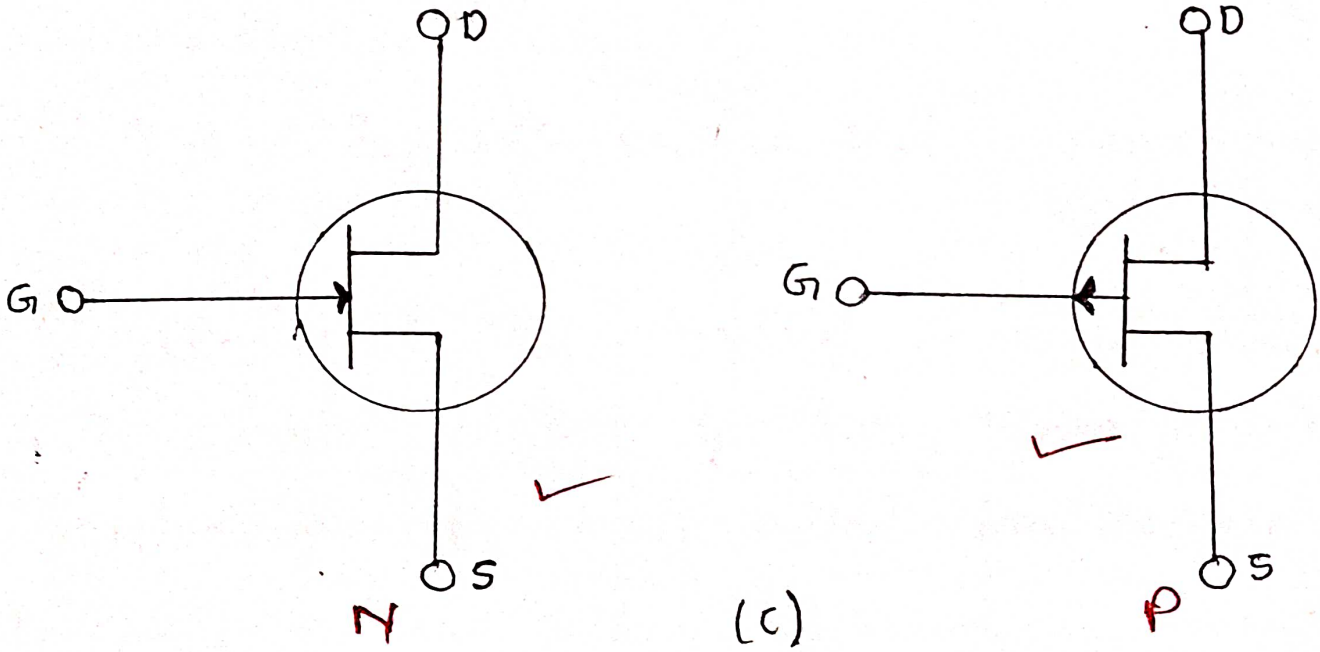
Construction :-

As shown in fig. it can be fabricated with either an N-channel or p-channel though N-channel is generally preferred. For fabricating an N-channel JFET, first a narrow bar of N-type semiconductor material is taken and then two P-type junctions are diffused on opposite sides of its middle part. These junction form two P-N diodes or gates and the area between these gates is called channel.





(b)



(c)

The two P-regions are internally connected and a single lead in brought out which is called gate terminal. ohmic contacts are made at the two ends of the bar - one lead is called source

terminal S and the other drain terminal when potential difference is established between drain and Source, current flows along the lenght of the bar through the channel located between the two P-regions. The current consists of only majority carriers which, in the present case, are electrons. P-channel FET is similar in construction except that it uses P-type bar and two N-type junctions.

Following FET notation is worth remembering

1. Source. It is the terminal through which majority carriers enter the bar. Since carrier come from it, it is called the Source.

2. Drain. It is the terminal through which majority carriers leave the bar. The drain-to-Source Voltage V_{DS} drives the drain current I_D

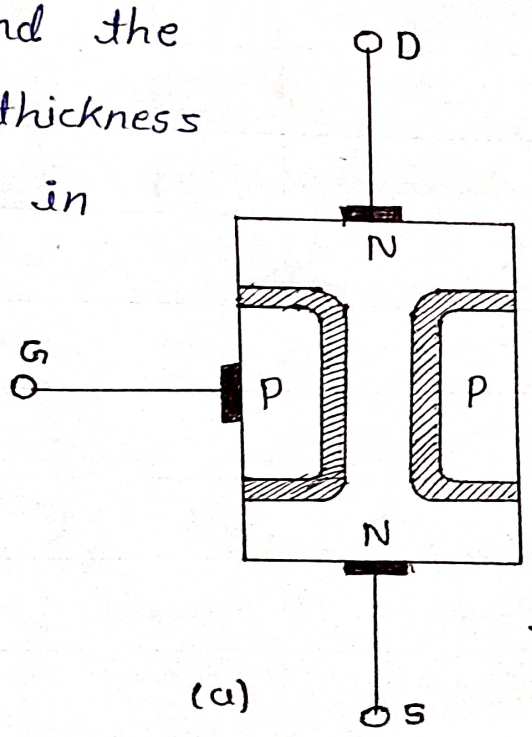
3. Gate. These are two internally-connected heavily-doped regions which form two P-N junctions. The gate-Source voltage V_{GS} reverse-biases the gates.

4. Channel. It is the space between two gates through which majority carriers pass from Source to drain when V_{DS} is applied.

Working And Opreation :-

(i) When $V_{GS} = 0$ and $V_{DS} = 0$

In this case, drain current $I_D = 0$, because $V_{DS} = 0$. The depletion regions around the P-junctions are of equal thickness and symmetrical as shown in fig. (a).



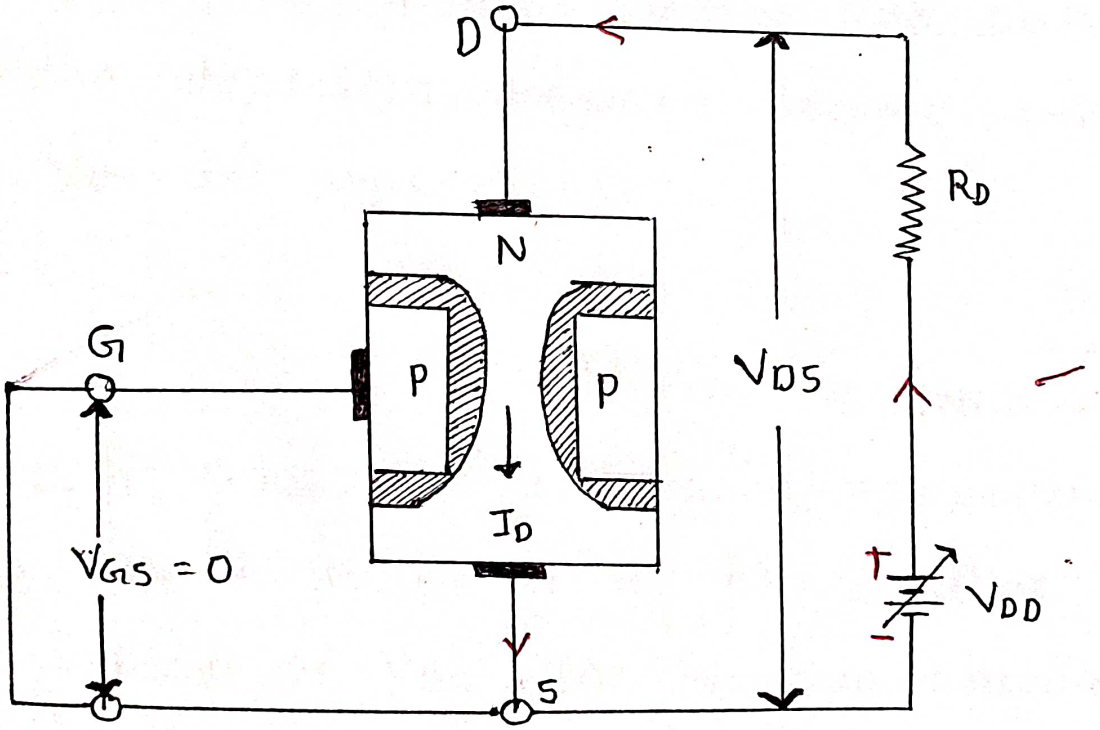
(a)

$V_{DS} = 0$

$V_{GS} = 0$

ii) When $V_{GS} = 0$ and V_{DS} is increased from zero

For this purpose, the JFET is connected to the V_{DD} supply as shown in fig. (b). The electrons flow from S to D, whereas conventional drain current I_D flows through the channel from D to S. Now, the gate-to-channel bias at any point along the channel is $= |V_{DS}| + |V_{GS}|$ i.e., the numerical sum of the two voltage. In the present case, external bias $V_{GS} = 0$.



$V_{DS} < V_{PO}$

$V_{GS} = 0$

(b)

Hence gate - channel reverse bias is provided by V_{DS} alone. Since the value of V_{DS} keeps decreasing as we go from D to S, the gate - channel bias also decreases accordingly. It has maximum value in the drain - gate region and minimum in the Source - gate region.

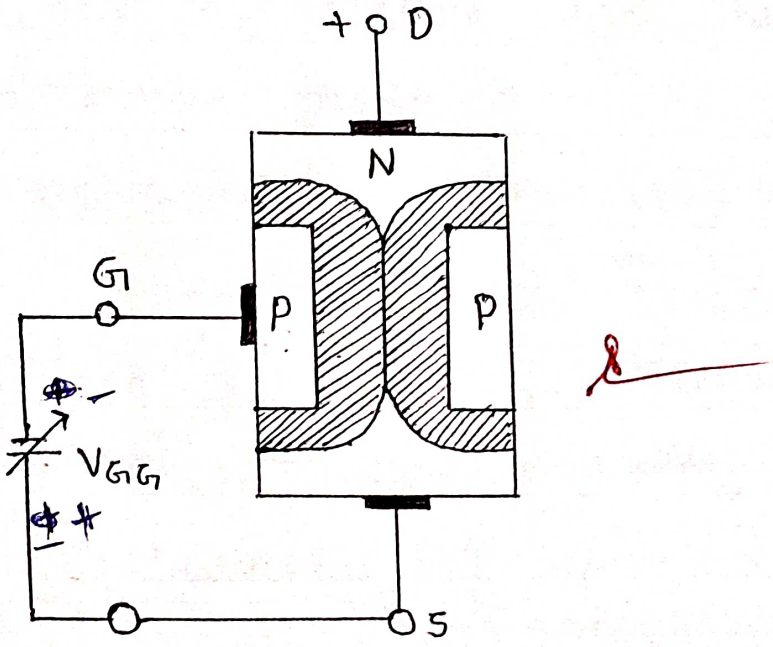
Hence, depletion regions penetrate more deeply into the channel in the drain - gate region than in the Source - gate region. This explains why the depletion regions become wedge shaped when V_{DS} is applied.

As V_{DS} is gradually increased from zero, I_D increases proportionally as per Ohm's law. It is found that for small initial values of V_{DS}, the N-type channel material acts like a resistor of constant value. It is so because V_{DS} being small, the depletion regions are not large enough to have any significant effect on channel cross - section and, hence,

its resistance. Consequently, I_D increases linearly as V_{DS} is increased from zero onwards.

(iii) when $V_{DS} = 0$ and V_{GS} is decreased from zero

In this case, as V_{GS} is made and more negative, the gate reverse bias increase which increases the thickness of the depletion region. As negative value of V_{GS} is increased, a stage comes when the two depletion regions touch each other as shown in fig.



(c) $|V_{GS(off)}| = |V_{PO}|$

$I_D = 0$

cut - off

In this condition, the channel is said to be cut-off. This value of V_{GS} which cuts of the channel and hence the drain current is called $V_{GS(off)}$.***

It may be noted that

$$\text{Or } |V_{PO}| = |V_{GS(off)}|.$$

because

$$V_{PO} = 4V, \quad V_{GS(off)} = -4V.$$

Obviously, the values are equal.

(iv) When V_{GS} is negative and V_{DS} is increased As V_{GS} is made more and more negative, of V_P as well as breakdown voltage V_B are decreased.

Since gate voltage controls the drain current, JFET is called a voltage-controlled device. A P-channel JFET operates in the same manner as an N-channel JFET except that current carriers are holes and polarities of both V_{DD} and V_{GS} are reversed.

Since only one type of majority carrier is used in JFET, they are called unlike bipolar junction transistors which use both electrons and holes as carries (and hence are called bipolar devices).

FET Parameters

1) Drain Resistance (r_d) :-

It is given by the relation of small change in drain to source voltage (ΔV_{DS}) to the corresponding change in Drain current (ΔI_D) for a constant gate to source voltage (ΔV_{GS}), when the JFET is operating in pinch-off region

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at a constant } V_{GS}$$

2) Trans Conductance (g_m) :-

Ratio of small change in drain current (ΔI_D) to the corresponding change

in gate to Source Voltage (ΔV_{GS}) for a constant V_{DS}.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

The value of g_m is expressed in mho's (Ω)

3) Amplification factor (μ) :-

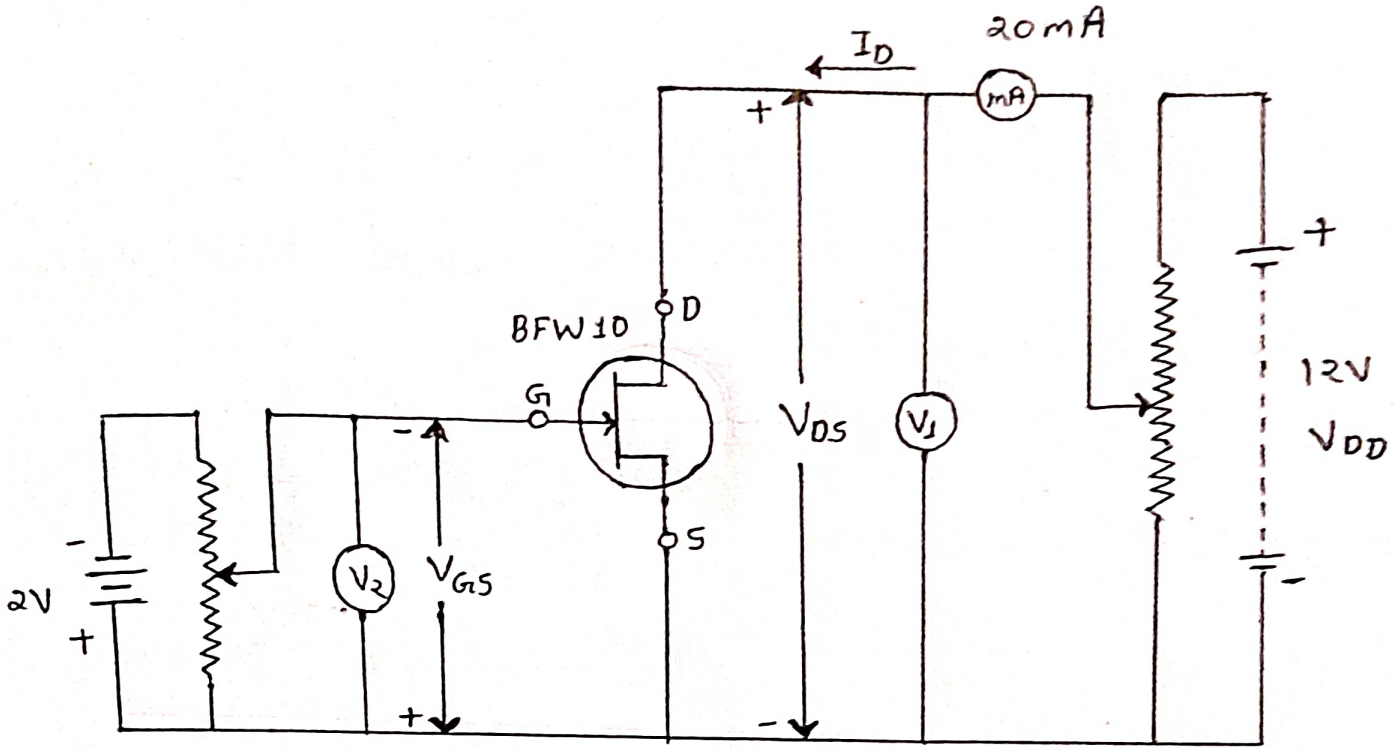
It is given by the ratio of small change in drain to Source Voltage (ΔV_{DS}) to the corresponding change in gate to Source Voltage (ΔV_{GS}) for a constant drain current (I_D).

$$\mu = \left(\frac{\Delta V_{DS}}{\Delta I_D}\right) \times \left(\frac{\Delta I_D}{\Delta V_{GS}}\right) = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

ie.

$$\mu = r_d \times g_m$$

Circuit Diagram :-



Procedure :-

Drain Characteristics :-

1) Connect the ~~Circit~~ circuit as shown in the figure.

2) Keep V_{GS} = 0V by varying V_{GG}.

3) Varying V_{DD} gradually in steps of 1V up to

10V note down drain current I_D and drain to source voltage (V_{DS}).

4) Repeat above procedure for V_{GS} = -0.4, -0.8, -1.2 and -1.6V

Transfer Characteristics :-

1) Connect the circuit as shown in the figure.

2) Set Voltage V_{DS} = 4V/8V

3) Varying V_{DS} in steps of 0.5V until the current I_D reduces to minimum value.

4) Varying V_{GG} gradually, note down both drain current I_D and gate - source Voltage (V_{GS}).

5) Repeat above procedure for V_{DS} = 4V/8V.

e of Preparation :

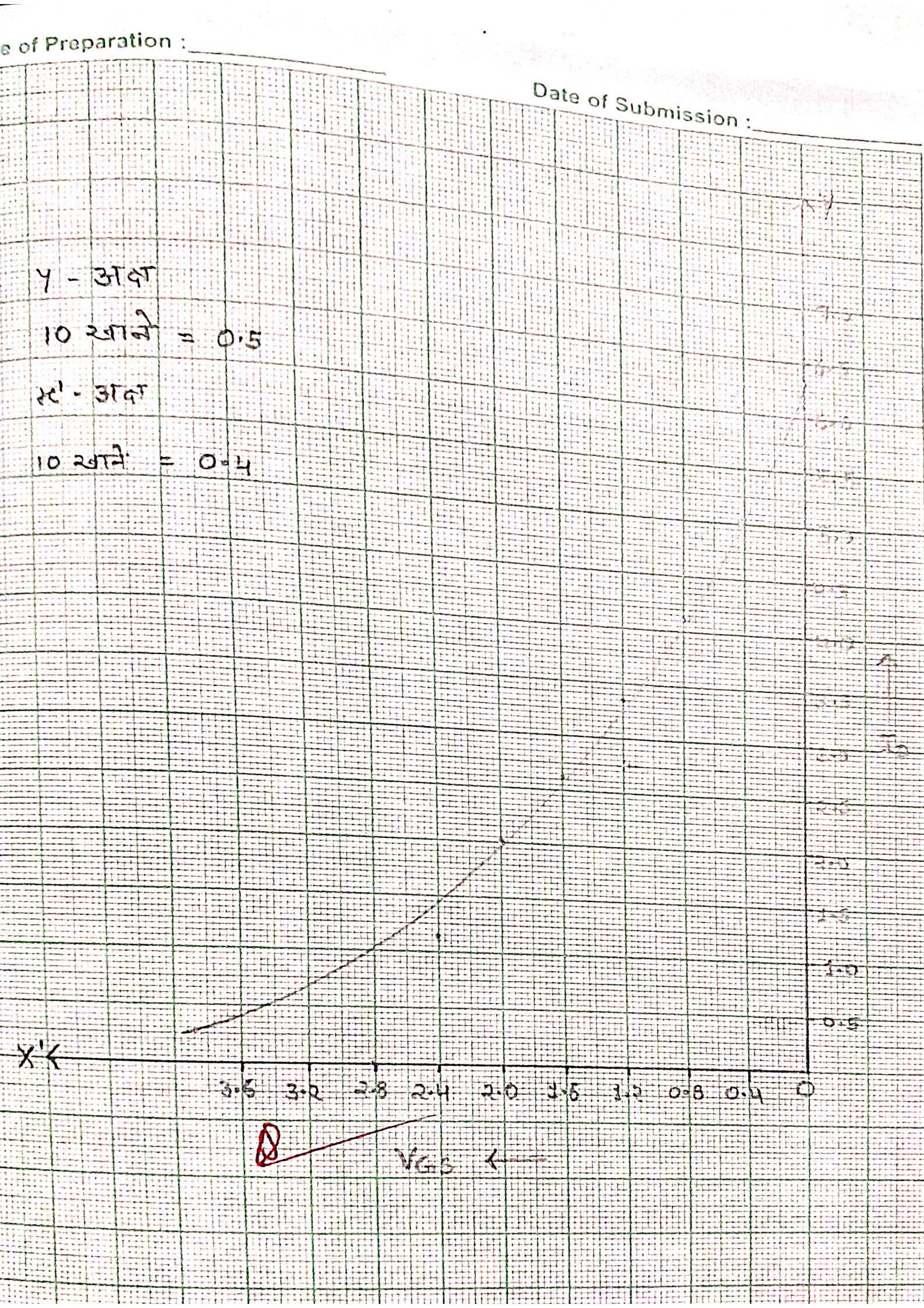
Date of Submission :

Y - अक्ष

10 खाने = 0.5

X' - अक्ष

10 खाने = 0.4



Observation Table :-

Transfer characteristics

S.No.	V_{GS} (Volt)	I_D (mA)
1.	0.0	6.39
2.	0.42	5.01
3.	0.81	4.10
4.	1.22	3.36
5.	1.65	2.62
6.	2.04	2.06
7.	2.4	1.12
8.	2.8	0.01
9.	3.2	0.0

Graph :-

Plot the transfer characteristics by taking V_{GS} on X-axis and taking I_D on Y-axis at constant V_{DS}.